CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 3 (canceled).

Claim 4 (previously presented). A method for fabricating a buried bit line for a semiconductor memory, which comprises:

producing strip-like doped regions parallel to and at distances from one another in a semiconductor body, the strip-like doped regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor;

applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer, a storage layer, and an upper boundary layer; and

forming an oxide region thicker than the lower boundary layer, in each case, on a side of the doped region remote from the semiconductor body;

before producing the upper boundary layer and after the application of the storage layer, applying a sacrificial layer with a topside to the storage layer;

producing openings with lateral walls in the sacrificial layer, the storage layer, and the lower boundary layer, by using a mask;

introducing dopant into implantation regions of the semiconductor body through the openings;

etching back the lateral walls of the openings and a topside of the sacrificial layer at an etching rate sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer;

removing residues of the sacrificial layer selectively with respect to the storage layer; and

producing the upper boundary layer on the storage layer and forming an oxide region on a free surface of the semiconductor body, in each case between the sides.

Claim 5 (original). The method according to claim 4, which further comprises heating until the dopant introduced into

the implantation regions has diffused to a portion of the semiconductor body covered by the storage layer.

Claim 6 (previously presented). The method according to claim 4, wherein the sacrificial layer is produced as a deposited oxide.

Claim 7 (previously presented). The method according to claim 4, which further comprises selecting the storage layer from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon.

Claim 8 (canceled).